Solid-State Image Pickup Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a solid-state image pickup apparatus having a photoelectric conversion function.

Related Background Art

Conventionally, a conventional solid-state image pickup apparatus extends the dynamic range by, e.g., reading out two kinds of signals with different accumulation periods from one pixel and combining the two kinds of signals, i.e., combining a signal having high sensitivity but narrow dynamic range with a signal having low sensitivity but wide dynamic range.

In this method, after signal charges are accumulated in a given accumulation period, signal charges must be accumulated again in another accumulation period. For this reason, image signals with different accumulation periods are obtained.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a solid-state image pickup apparatus capable of extending the dynamic range and a signal read-out method for the solid-state image pickup apparatus.

In order to achieve the above object, according to

an aspect of the present invention, there is provided a solid-state image pickup apparatus comprising:

a photoelectric conversion unit;

transfer means for transferring signal charges from the photoelectric conversion unit;

capacitance means for holding the transferred signal charges; and

amplification means for outputting a signal corresponding to the signal charges held by the capacitance means,

wherein the capacitance means having a capacitance unit includes a first capacitance value and an additive capacitance unit for adding a capacitance to the capacitance unit to increase the first capacitance value to obtain a second capacitance value, and

wherein a signal read-out from the amplification means has a first read-out mode in which a signal is read out while holding the signal charges in the capacitance unit and the additive capacitance unit, and a second read-out mode in which a signal is read out while holding the signal charges in the capacitance unit.

According to another aspect, there is provided a signal read-out method for a solid-state image pickup apparatus which holds, in capacitance means, signal charges generated by a photoelectric conversion unit and outputs a signal corresponding to the signal

charges held by the capacitance means from amplification means, comprising

a first read-out mode in which a signal is output from the amplification means while holding the signal charges generated by the photoelectric conversion unit in the capacitance means set at a first capacitance value, and

a second read-out mode in which, after the first read-out mode, the capacitance value of the capacitance means is changed from the first capacitance value to a second capacitance value, and a signal corresponding to the signal charges held by the capacitance means set at the second capacitance value is output from the capacitance means.

According to still another aspect, there is provided a solid-state image pickup apparatus comprising:

a photoelectric conversion unit; and

a charge/voltage conversion unit for converting signal charges transferred from the photoelectric conversion unit into a signal voltage,

wherein the charge/voltage conversion unit comprises a plurality of capacitances having different dependences on voltage.

According to still another aspect, there is provided a solid-state image pickup apparatus including a plurality of pixels, each pixel comprising:

a photoelectric conversion unit;

holding means for holding a signal from the photoelectric conversion unit;

read-out means for reading out the signal held by the holding means; and

capacitance changing means for changing a capacitance value of the holding means.

According to still another aspect, there is provided a solid-state image pickup apparatus including a plurality of pixels, each pixel comprising:

a photoelectric conversion unit;

a charge/voltage conversion unit for generating a voltage corresponding to a charge amount of the signal charges from the photoelectric conversion unit;

control means for controlling to change a charge/voltage conversion efficiency of the charge/voltage conversion unit in accordance with the charge amount of the signal charges; and

read-out means for reading out the voltage generated by the charge/voltage conversion unit to an output line.

According to still another aspect, there is provided a solid-state image pickup apparatus including a plurality of pixels, each pixel comprising:

a photoelectric conversion unit;

a charge/voltage conversion unit for generating a voltage corresponding to a charge amount of the signal

charges from the photoelectric conversion unit; and

read-out means for reading out the voltage generated by the charge/voltage conversion unit to an output line,

wherein a charge/voltage conversion efficiency of the charge/voltage conversion unit changes in accordance with the charge amount of the signal charges.

The above and other objects, features, and advantages of the present invention will be apparent from the following detailed description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view showing a solid-state image pickup apparatus;

Fig. 2 is a timing chart showing the operation of the solid-state image pickup apparatus shown in Fig. 1;

Fig. 3 is a graph showing the photoelectric conversion characteristics of the solid-state image pickup apparatus shown in Fig. 1;

Figs. 4A, 4B, 4C and 4D are potential charts showing the read-out operation of the solid-state image pickup apparatus shown in Fig. 1;

Fig. 5 is a timing chart showing another signal read-out method for the solid-state image pickup apparatus;

Fig. 6 is a schematic view showing a pixel of another solid-state image pickup apparatus;

Fig. 7 is a timing chart showing the operation of the solid-state image pickup apparatus shown in Fig. 6;

Fig. 8 is a graph showing the photoelectric conversion characteristics of the solid-state image pickup apparatus shown in Fig. 6;

Fig. 9 is a schematic view showing still another solid-state image pickup apparatus;

Fig. 10 is a timing chart showing the operation of the solid-state image pickup apparatus shown in Fig. 9;

Figs. 11A, 11B, 11C and 11D are potential charts for explaining the operation of the solid-state image pickup apparatus shown in Fig. 9;

Fig. 12 is a schematic view showing still another solid-state image pickup apparatus;

Fig. 13 is a timing chart showing the operation of the solid-state image pickup apparatus shown in Fig. 12;

Fig. 14 is an explanatory view showing the structure of a pixel of a solid-state image pickup element;

Fig. 15 is a timing chart showing the operation of the solid-state image pickup element shown in Fig. 14;

Fig. 16 is a schematic view showing the structure of an area sensor;

Fig. 17 is a timing chart of the area sensor;

Fig. 18 is a schematic view showing still another solid-state image pickup apparatus;

Fig. 19 is a schematic view showing still another solid-state image pickup apparatus;

Fig. 20 is a timing chart showing the signal read-out method for the solid-state image pickup apparatus;

Fig. 21 is a schematic explanatory view showing the arrangement of still another solid-state image pickup apparatus;

Fig. 22 is a schematic explanatory view showing the arrangement of still another solid-state image pickup apparatus;

Figs. 23A, 23B and 23C are explanatory views of FD and MOS structure units having a staircase potential structure;

Figs. 24A, 24B and 24C are graphs showing the VFD vs. Q characteristics, VFD vs. Cap characteristics, and light amount vs. output characteristics, respectively;

Figs. 25A, 25B and 25C are explanatory views of FD and MOS structure units having an inverted "U"-shaped potential structure;

Figs. 26A, 26B and 26C are graphs showing the VFD vs. Q characteristics, VFD vs. Cap characteristics, and light amount vs. output characteristics, respectively;

Fig. 27 is a schematic plan view of a solid-state image pickup apparatus having a MOS capacitance;

Fig. 28 is a schematic plan view of another solid-state image pickup apparatus having a MOS capacitance;

Fig. 29 is a schematic sectional view showing an FD region and buried p-n junction;

Fig. 30 is a graph showing the relationship between a reverse bias voltage and capacitance;

Fig. 31 is a schematic sectional view showing an FD region and buried p-n junction;

Fig. 32 is a schematic plan view of a solid-state image pickup apparatus having a buried p-n junction;

Fig. 33 is a plan view showing the planar shape of an n-type diffusion region when a staircase potential structure is formed;

Fig. 34 is a plan view showing the planar shape of an n-type diffusion region when an inverted "U"-shaped potential structure is formed;

Fig. 35 is a schematic view of a solid-state image pickup apparatus including a reset MOS transistor;

Figs. 36A, 36B, 36C and 36D are potential charts showing the light accumulation operation, reset operation, noise read-out operation, and signal transfer/signal read-out operation, respectively;

Figs. 37A and 37B are potential charts showing an operation of changing the reset potential to change the sensitivity;

Fig. 38 is a graph showing the light amount vs.

output characteristics (sensitivity characteristics);

Fig. 39 is a view showing a pixel structure so as to explain the reset voltage application method;

Fig. 40 is a view showing another pixel structure so as to explain the reset voltage application method;

Fig. 41 is a view showing still another pixel structure so as to explain the reset voltage application method;

Fig. 42 is a block diagram of a camera apparatus using a solid-state image pickup apparatus which sets the reset voltage in accordance with a sampling result;

Fig. 43 is a potential chart for explaining a sampling signal detection operation;

Fig. 44 is a schematic view showing the structure of another area sensor;

Fig. 45 is a block diagram showing a solid-state image pickup apparatus according to the 11th embodiment of the present invention;

Fig. 46 is a timing chart showing the operation of the solid-state image pickup apparatus of the 11th embodiment;

Fig. 47 is a graph showing the VFD vs. Cap characteristics;

Fig. 48 is a block diagram showing a video camera apparatus according to the present invention; and

Fig. 49 is a block diagram showing a conventional video camera apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below with reference to the accompanying drawings.

Fig. 1 is a schematic view showing a solid-state image pickup apparatus according to the first embodiment of the present invention.

Referring to Fig. 1, one pixel cell is constructed by a photodiode PD, transfer switch MTX, reset switch MRES, selection switch MSEL, amplification means MSF, capacitance CFD, and MOS inverted capacitance Cox. The capacitance CFD is the capacitance of a floating diffusion to which signal charges are transferred and is constituted by a parasitic capacitance generated by a MOS source-drain junction capacitance or line capacitance. The MOS inverted capacitance Cox is generated by a voltage applied to the gate and added to the capacitance CFD as needed. Each of the switches and amplification means is constructed by a MOS transistor. This pixel is used for an area sensor and therefore has the selection switch MSEL. A line sensor need not have the selection switch MSEL.

The amplification means MSF is connected to capacitances CTN1, CTN2, CTS1, and CTS2 through change-over switches MTN1, MTN2, MTS1, and MTS2. The capacitances CTN1 and CTN2 are connected to the inverting input terminal (-) of a differential

amplifier A through common output means MTH1 and MTH2. The capacitances CTS1 and CTS2 are connected to the noninverting input terminal (+) of the differential amplifier A through common output means MTH3 and MTH4. Signals ϕTX, ϕRES, ϕSEL, ϕTN1, ϕTN2, ϕTS1, and ϕTS2 control the transfer switch MTX, reset switch MRES, selection switch MSEL, and switching means MTN1, MTN2, MTS1, and MTS2, respectively. A control signal ϕcap forms the MOS inverted capacitance Cox. A signal ϕTH controls the common output means MTH1, MTH2, MTH3, and MTH4.

The operation of the solid-state image pickup apparatus will be described next with reference to the timing chart in Fig. 2.

First, the signal ϕRES is set at high level to turn on the reset switch MRES and reset the gate of the amplification means MSF. The capacitance Cox is not added because the signal ϕcap is at low level. The capacitance CFD is added to the gate of the amplification means. In this state, the signals ϕSEL and ϕTN1 are set at high level to turn on the selection switch MSEL and change-over switch MTN1. A noise signal N1 after reset is read out from the amplification means MSF and accumulated in the capacitance CTN1 (first noise read-out).

Next, the signal ϕcap is set at high level to add the capacitance Cox to the capacitance CFD. In this

state, the signals φSEL and φTN2 are set at high level to turn on the selection switch MSEL and change-over switch MTN2. A noise signal N2 is read out from the amplification means MSF and accumulated in the capacitance CTN2 (second noise read-out). With this operation, noise signals are read out and accumulated while adding different capacitances to the gate of the amplification means MSF.

After that, the signal φTX is set at high level to transfer signal charges from the photodiode PD. While keeping the signal φcap at high level and the capacitance Cox added to the capacitance CFD, the signals φSEL and φTS1 are set at high level to turn on the selection switch MSEL and change-over switch MTS1. A sensor signal S1 containing the noise signal N2 is read out from the amplification means MSF and accumulated in the capacitance CTS1 (first signal read-out). The signal φcap is set at low level to remove the capacitance Cox while keeping the capacitance CFD added to the gate of the amplification means MSF. In this state, the signals φSEL and φTS2 are set at high level to turn on the selection switch MSEL and change-over switch MTS2. A sensor signal S2 containing the noise signal N1 is read out from the amplification means MSF and accumulated in the capacitance CTS2 (second signal read-out). With this operation, two sensor signals having different dynamic

ranges can be obtained on the basis of signals charges accumulated in the same accumulation period.

Next, the signal ϕTH is set at high level to read out the sum of the noise signals N1 and N2 from the capacitances CTN1 and CTN2 through the common line and read out the sum of the sensor signals S1 and S2 from the capacitances CTS1 and CTS2 through the common line. The differential amplifier calculates (S1 + S2) - (N1 + N2). A resultant signal exhibits photoelectric conversion characteristics shown in Fig. 3. As shown in Fig. 3, the output (S1 + S2) - (N1 + N2) corresponds to the sum of a signal (S1 - N2) and a signal (S2 - N1).

The above-described read-out operation will be described with reference to the potential charts in Figs. 4A to 4D.

Fig. 4A is a potential chart in the first noise read-out. The noise (N1) is read out while adding the capacitance CFD without the capacitance Cox. Since the transfer switch is OFF, and the barrier is high, the signal charges are accumulated in the photodiode PD. Fig. 4B is a potential chart in the second noise read-out. The noise (N2) is read out while forming the capacitance Cox and adding it to the capacitance CFD. Fig. 4C is a potential chart in the first signal read-out. At this time, the transfer switch is turned on to transfer the signal charges from the photodiode

PD to the capacitances CFD and Cox. The sensor signal (S1) is read out while accumulating the signal charges in the capacitances CFD and Cox. Fig. 4D is a potential chart in the second signal read-out. At this time, the capacitance Cox disappears, and the signal charges are transferred and accumulated in the capacitance CFD. In this state, the sensor signal (S2) is read out. With this operation, the first and second noise signals and first and second sensor signals are read out on the basis of the different capacitances.

Fig. 5 is a timing chart showing another signal read-out method of the present invention. As shown in Fig. 5, first, the gate is reset while keeping the signal ϕcap at high level. A noise signal N11 is read out from the amplification means MSF while keeping the signal ϕcap at high level to add the capacitance Cox to the capacitance CFD. Next, the signal ϕcap is set at low level to remove the capacitance Cox. A noise signal N12 is read out from the amplification means MSF without adding the capacitance Cox to the capacitance CFD at the gate of the amplification means MSF.

After that, the signal ϕcap is set at high level to add the capacitance Cox to the capacitance CFD. In this state, a sensor signal S11 containing the noise signal N11 is read out from the amplification means MSF. Next, the signal ϕcap is set at low level to remove the capacitance Cox. A sensor signal S12

containing the noise signal N12 is read out from the amplification means MSF without adding the capacitance Cox to the capacitance CFD.

This signal read-out method is different from that shown in Fig. 2 in that after the noise is read out while adding the capacitance Cox, the noise is read out without adding the capacitance Cox. In this method, the signal ϕcap changes from high level to low level in both the noise read-out period and the signal read-out period. For this reason, the influence of characteristics due to the level change in the signal ϕcap can be constant. The influence of the level change in signal ϕcap can be eliminated by calculating (S1 + S2) - (N1 + N2).

In the first embodiment, one MOS inverted capacitance is prepared as the additive capacitance unit. However, a plurality of MOS inverted capacitances may be used.

In the second embodiment, two MOS inverted capacitances are prepared. Fig. 6 is a schematic view showing a pixel of a solid-state image pickup apparatus according to the second embodiment of the present invention. Fig. 7 is a timing chart showing the operation of the apparatus. Fig. 8 is a graph showing the photoelectric conversion characteristics.

The pixel structure shown in Fig. 6 is different from that in Fig. 1 in that MOS inverted capacitances

Cox1 and Cox2 are connected in parallel, and the capacitance Cox1 or/and capacitance Cox2 can be added to a capacitance CFD in accordance with signals ϕcap1 and ϕcap2. The remaining parts are the same as in Fig. 1.

As for the operation of this solid-state image pickup apparatus, first, a signal ϕRES is set at high level to turn on a reset switch MRES and reset the gate of an amplification means MSF, as shown in the timing chart of Fig. 7. The inverted capacitances Cox1 and Cox2 are not added because the signals ϕcap1 and ϕcap2 are at low level, and the capacitance CFD is added to the gate of the amplification means MSF. In this state, a signal ϕSEL is set at high level to turn on a selection switch MSEL and read out a noise signal N1 from the amplification means MSF (first noise read-out).

Next, the signal ϕcap1 is set at high level to add the inverted capacitance Cox1 to the capacitance CFD. In this state, the signal ϕSEL is set at high level to turn on the selection switch MSEL and read out a noise signal N2 from the amplification means MSF (second noise read-out). The signal ϕcap2 may be set at high level to add the capacitance Cox2 to the capacitance CFD.

After that, the signal ϕcap1 is kept at high level, and the signal ϕcap2 is set at high level to add

the inverted capacitances Cox1 and Cox2 to the capacitance CFD. In this state, the signal ϕSEL is set at high level to turn on the selection switch MSEL and read out a noise signal N3 from the amplification means MSF (third noise read-out).

A signal ϕTX is set at high level to transfer signal charges from a photodiode PD. The signals ϕcap1 and ϕcap2 are kept at high level to add the inverted capacitances Cox1 and Cox2 to the capacitance CFD. In this state, the signal ϕSEL is set at high level to turn on the selection switch MSEL and read out a sensor signal S1 containing the noise signal N3 from the amplification means MSF (first signal read-out).

Next, the signal ϕcap2 is set at low level to remove the capacitance Cox2. While keeping the capacitance CFD and capacitance Cox1 added to the gate of the amplification means MSF, the signal ϕSEL is set at high level to turn on the selection switch MSEL and read out a sensor signal S2 containing the noise signal N2 from the amplification means MSF (second signal read-out).

The signal ϕcap2 is kept at low level, and the signal ϕcap1 is set at low level to remove the inverted capacitances Cox1 and Cox2 while adding the capacitance CFD to the gate of the amplification means MSF. In this state, the signal ϕSEL is set at high level to turn on the selection switch MSEL and read out a sensor

signal S3 containing the noise signal N1 from the amplification means MSF (third signal read-out).

The readout noise signals N1 to N3 and sensor signals S1 to S3 are accumulated in corresponding capacitances. The noise signals N1 to N3 are added and input to the inverting input terminal (-) of the differential amplifier. The sensor signals S1 to S3 are added and input to the noninverting input terminal (+) of the differential amplifier. The differential amplifier calculates (S1 + S2 + S3) - (N1 + N2 + N3). A resultant signal exhibits photoelectric conversion characteristics shown in Fig. 8. As shown in Fig. 8, the output (S1 + S2 + S3) - (N1 + N2 + N3) corresponds to the sum of a signal (S1 - N3), a signal (S2 - N2), and a signal (S3 - N1).

According to this embodiment, a sensor signal having a wider dynamic range can be obtained on the basis of signal charges accumulated in the same accumulation period.

The same signal read-out method as that described in the first embodiment with reference to Fig. 5 can be used for this embodiment. Fig. 20 is a timing chart showing the signal read-out method. As shown in Fig. 20, the levels of the signals ϕcap1 and ϕcap2 are changed in the same direction (from low level to high level) in the noise read-out period and signal read-out period. For this reason, the influence of the

characteristics due to the level change in signals ϕcap1 and ϕcap2 can be constant. The influence of the level change in signals ϕcap1 and ϕcap2 can be eliminated by calculating (S1 + S2 + S3) - (N1 + N2 + N3).

In the first and second embodiments, the inverted MOS capacitance is provided to add a capacitance to the capacitance CFD. However, the capacitance to be added to the capacitance CFD can be formed without preparing any element for adding the capacitance.

In the third embodiment, the channel of a MOS transistor serving as a transfer switch is used as a capacitance. Fig. 9 is a schematic view showing a solid-state image pickup apparatus according to the third embodiment of the present invention. Fig. 10 is a timing chart showing the operation of the apparatus. Figs. 11A to 11D are potential charts for explaining the operation of the apparatus.

The pixel structure shown in Fig. 9 is different from that in Fig. 1 in that the MOS inverted capacitance Cox is not arranged. In this embodiment, the channel of a MOS transistor MTX serving as a transfer switch is used as a capacitance.

The operation will be described with reference to Figs. 10 and 11A to 11D.

First, a signal ϕRES is set at high level to turn on a reset switch MRES and reset the gate of an

amplification means MSF. After that, signals ϕSEL and ϕTN are set at high level to turn on a selection switch MSEL and change-over switches MTN1 and MTN2. A noise signal N is read out from the amplification means MSF and accumulated in capacitances CTN1 and CTN2 (noise read-out). Fig. 11A is a potential chart of this operation.

A signal ϕTX is set at high level to transfer signal charges from a photodiode PD. While keeping the signal ϕTX at high level, the signals ϕSEL and ϕTS1 are set at high level to turn on the selection switch MSEL and change-over switch MTS1. A sensor signal S1 containing the noise signal is read out from the amplification means MSF and accumulated in a capacitance CTS1. When the signal ϕTX is at high level, the channel of the MOS transistor MTX serving as a transfer switch functions as a capacitance (inverted capacitance). This capacitance is called a capacitance CTX. As shown in the potential chart of Fig. 11B, the capacitance CTX is added to a capacitance CFD. The sensor signal S1 is read out while keeping the signal charges accumulated in both capacitances.

To remove the capacitance CTX, the level of the signal ϕTX is lowered. At this time, the signal ϕTX is temporarily set at middle level to prevent the signal charges from flowing to the photodiode PD side and transfer all charges to the capacitance CFD side. In

the potential chart of Fig. 11C, the signal ϕTX is set at middle level to transfer all charges to the capacitance CFD side.

The signal ϕTX is changed from middle level to low level. While keeping the signal charges accumulated in the capacitance CFD, the signals ϕSEL and ϕTS2 are set at high level to turn on the selection switch MSEL and change-over switch MTS2. A sensor signal S2 containing the noise signal is read out from the amplification means MSF and accumulated in the capacitance CTS2. In the potential chart of Fig. 11D, the signal ϕTX is set at low level, and all charges are accumulated on the capacitance CFD side.

Next, the signal ϕTH is set at high level to read out the sum of the noise signals N from the capacitances CTN1 and CTN2 through the common line and the sum of the sensor signals S1 and S2 from the capacitances CTS1 and CTS2 through the common line. The differential amplifier calculates (S1 + S1) - (2N).

According to this embodiment, a simpler pixel structure can be realized.

In the first and second embodiments, the inverted MOS capacitance is provided to add a capacitance to the capacitance CFD. Two transfer switches may be provided, and a capacitance may be formed between the first transfer switch and the second transfer switch as an additive capacitance.

In the fourth embodiment, two transfer switches are prepared, and an additive capacitance is formed therebetween. The number of transfer switches is not limited to two. Three or more transfer switches may be provided (two or more additive capacitances are formed accordingly). Fig. 12 is a schematic view showing a solid-state image pickup apparatus according to the fourth embodiment of the present invention. Fig. 13 is a timing chart showing the operation of the apparatus.

The pixel structure shown in Fig. 12 is different from that in Fig. 1 in that two MOS transistors MTX1 and MTX2 are prepared as transfer switches, a capacitance CFD1 is formed between the MOS transistor MTX1 and MOS transistor MTX2. The capacitance added to the gate of an amplification means MSF is switched between a capacitance CFD2 and a capacitance (CFD1 + CFD2) by controlling signals ϕTX1 and ϕTX2. The remaining parts are the same as those of the pixel structure shown in Fig. 1.

The operation of this solid-state image pickup apparatus will be described next with reference to the timing chart in Fig. 13.

First, a signal ϕRES is set at high level to turn on a transistor MRES and reset the gate of the amplification means MSF. The signal ϕTX2 is kept at high level, and the capacitance CFD1 is added to the capacitance CFD2. In this state, signals ϕSEL and ϕTN1

are set at high level to turn on a selection switch MSEL and change-over switch MTN1. A noise signal N1 is read out from the amplification means MSF and accumulated in a capacitance CTN1 (first noise read-out).

The signal ϕTX2 is at low level, and the capacitance CFD2 is added to the gate of the amplification means MSF (the capacitance CFD1 is not added). In this state, the signals ϕSEL and ϕTN2 are set at high level to turn on the selection switch MSEL and change-over switch MTN2. A noise signal N2 is read out from the amplification means MSF and accumulated in the capacitance CTN2 (second noise read-out). With this operation, noise signals can be read out and accumulated while adding different capacitances to the gate of the amplification means after reset.

After that, the signals ϕTX2 and ϕTX1 are set at high level to transfer signal charges from a photodiode PD to the capacitances CFD1 and CFD2. The signal ϕTX1 is set at low level, and the signal ϕTX2 is kept at high level. While keeping the capacitance CFD1 added to the capacitance CFD2, the signals ϕSEL and ϕTS1 are set at high level to turn on the selection switch MSEL and change-over switch MTS1. A sensor signal S1 containing the noise signal N1 is read out from the amplification means MSF and accumulated in a capacitance CTS1 (first signal read-out).

Next, the signal $\phi TX2$ is set at low level to disconnect the capacitance CFD1 (signal charges accumulated in the capacitance CFD1 are transferred to the capacitance CFD2 side). While keeping the capacitance CFD2 added to the gate of the amplification means MSF, the signals ϕSEL and $\phi TS2$ are set at high level to turn on the selection switch MSEL and change-over switch MTS2. A sensor signal S2 containing the noise signal N2 is read out from the amplification means MSF and accumulated in the capacitance CTS2 (second signal read-out).

A signal ϕTH is set at high level to read out the sum of the noise signals N1 and N2 from the capacitances CTN1 and CTN2 through the common line and the sum of the sensor signals S1 and S2 containing the noise signals N1 and N2, respectively, from the capacitances CTS1 and CTS2 through the common line. A differential amplifier A calculates (S1 + S2) - (N1 + N2).

A solid-state image pickup apparatus having two transfer switches is disclosed in Japanese Patent Publication No. 7-105915. Fig. 14 is an explanatory view showing the structure of a pixel of a solid-state image pickup element shown in Fig. 3 of Japanese Patent Publication No. 7-105915. Fig. 15 is a timing chart shown as Fig. 4 of this prior art.

As shown in Fig. 14, the solid-state image pickup

apparatus disclosed in Japanese Patent Publication No. 7-105915 also has transistors 26 and 28 for transferring signal charges from a photodiode 14 to the gate of a transistor 30.

In the solid-state image pickup apparatus disclosed in Japanese Patent Publication No. 7-105915, however, signals ϕ-1 and ϕ-2 are simultaneously set at high level to simultaneously turn on the transistors 26 and 28 to transfer signal charges, as shown in the timing chart of Fig. 15. This is different from the fourth embodiment shown in Fig. 13 in which the signals ϕTX1 and ϕTX2 are appropriately switched to turn on the transistors MTX1 and MTX2, change the capacitance to be added to the amplification means MSF, and output signals with different dynamic ranges.

In the first to fourth embodiments, one pixel cell has been described. In the fifth embodiment to be described below, the present invention is applied to an area sensor. Although an area sensor using the pixel cell shown in Fig. 1 will be described below, the pixels of the second to fourth embodiments can also be used. The pixel structure and the circuit arrangement of the read system are the same as in Fig. 1, and a detailed description thereof will be omitted.

Fig. 16 is a schematic view showing the structure of an area sensor. As shown in Fig. 16, rows of pixel cells arrayed in a matrix are scanned by a vertical

scanning circuit 100. Signals ϕRES, ϕTX, ϕSEL, and ϕcap are sent in units of rows. Noise and sensor signals are output to the vertical output lines and accumulated in corresponding capacitances in units of rows. The first and second noise signals and first and second sensor signals accumulated in the capacitances are scanned by a horizontal scanning circuit 101 in units of columns. The sum of the noise signals (N1 + N2) and the sum of the sensor signals (S1 + S2) are sequentially sent to the inverting input terminal (-) and noninverting input terminal (+) of a differential amplifier A in units of columns through the horizontal output lines. The differential amplifier A executes subtraction to obtain the signal (S1 + S2) - (N1 + N2) for each pixel. MOS transistors MCHR1 and MCHR2 for resetting the horizontal output lines to predetermined potentials are controlled by a signal ϕCHR.

Fig. 17 is a timing chart of the area sensor. This operation is the same as in Fig. 5, and a detailed description thereof will be omitted.

In the first embodiment, after the noise signals and sensor signals are added, respectively, the sum of noise signals is subtracted from the sum of sensor signals to output a signal. In the sixth embodiment, only subtraction for removing noise is performed without any addition, and a sensor signal (from which noise is removed) having a different dynamic range is

selected in accordance with an output selection signal from the system side.

Fig. 18 is a schematic view showing a solid-state image pickup apparatus according to the sixth embodiment of the present invention. The solid-state image pickup apparatus shown in Fig. 18 is different from that shown in Fig. 1 in the following point. In this embodiment, a noise signal N1 read out from a capacitance CTN1 and a sensor signal S2 read out from a capacitance CTS2 and containing the noise signal N1 are input to a differential amplifier A1, and S2 - N1 is calculated to output a signal. On the other hand, a noise signal N2 read out from a capacitance CTN2 and a sensor signal S1 read out from a capacitance CTS1 and containing the noise signal N2 are input to a differential amplifier A2, and S1 - N2 is calculated to output a signal. A selection means comprising two analog switches and an inverter is switched on the basis of an output selection signal to selectively output one of the signal (S2 - N1) and the signal (S1 - N2).

The present invention can be used not only to an area sensor but also to a line sensor. This will be described as the seventh embodiment. A line sensor has the same pixel structure as described above except that each pixel has no selection switch. Fig. 19 is a schematic view of a line sensor. The basic structure

of the line sensor is the same as that of the area sensor shown in Fig. 16.

As described above, according to the first to seventh embodiments, image signals having different dynamic ranges can be obtained using signal charges accumulated in the same accumulation period.

More specifically, a signal having high sensitivity but narrow dynamic range and a signal having low sensitivity but wide dynamic range can be obtained. In this case, the signal having high sensitivity but narrow dynamic range and the signal having low sensitivity but wide dynamic range can be selectively output as needed. For example, the signal can be selected on the basis of the luminance signal level.

The solid-state image pickup apparatuses of the first to seventh embodiments can be used for, e.g., back light correction.

Fig. 21 is a schematic explanatory view showing the arrangement of a solid-state image pickup apparatus according to the eighth embodiment. Referring to Fig. 21, the solid-state image pickup apparatus has an n-type semiconductor substrate 1, p-type well region 2 formed in the n-type semiconductor substrate 1, n-type diffusion region 3, and p-type region 4 formed on the surface of the n-type diffusion region 3. The p-type well region 2, n-type diffusion region 3, and p-type

region 4 form a photodiode. Signal charges accumulated in the photodiode are transferred to a charge/voltage conversion unit 5. This charge/voltage conversion unit is formed from an impurity diffusion region. Voltage conversion is achieved by all capacitances connected to this node. This region is generally called a floating diffusion (FD) region, including all capacitance components.

A transfer gate electrode 6 transfers signal charges from the photodiode to the FD region 5. The n-type diffusion region 3 and FD region 5 serve as the source and drain regions of a transfer MOS transistor (MTX), respectively. The FD region 5 is electrically connected to the gate of an output MOS transistor MSF and the drain of a reset MOS transistor MRES. The drain of the MOS transistor MSF is connected to the source of a MOS transistor MSEL serving as a selection switch, and the source of the MOS transistor MSF is connected to a constant current source, thereby forming a source follower circuit. When the signal charges transferred to the FD region 5 are applied to the gate of the MOS transistor MSF as a voltage signal, a signal is output from the source follower circuit. When the reset MOS transistor MRES is turned on, the FD region 5 is set at the reset potential.

The FD region 5 has a capacitance formed by the junction capacitance or line capacitance with respect

to the p-type well region 2. As shown in Fig. 22, MOS structure units 7 and 8 are series-connected to the FD region 5, so the MOS capacitances are connected to the capacitance of the FD region 5. In this case, the MOS capacitances are series-connected. However, the MOS capacitances may be connected in parallel.

The FD region 5 and MOS structure units 7 and 8 construct a charge/voltage conversion unit. The capacitances of the MOS structure units 7 and 8 can be set to have a dependence on voltage, which is different from that of the FD region, by adjusting the well density, gate oxide layer thickness, or a fixed voltage to be applied to the gate electrode. Although the capacitance formed by the junction capacitance or line capacitance between the FD region 5 and p-type well region 2 actually has a dependence on voltage, the capacitance change is small within the use range.

Figs. 23A to 23C are explanatory views of the FD region and MOS structure units which have a staircase potential structure. Figs. 24A is a graph showing the VFD (floating diffusion voltage) vs. Q (signal charge amount) characteristics. Fig. 24B is a graph showing the VFD vs. Cap (capacitance) characteristics. Fig. 24C is a graph showing the light amount vs. output characteristics (sensitivity characteristics). Symbols a, b, and c in Figs. 24A to 24C denote the characteristics corresponding to the operative states

shown in Figs. 23A to 23C, respectively. This potential structure can be obtained by connecting the MOS capacitances in series or parallel.

Referring to Figs. 23A to 23C, this structure has a photodiode unit PD, transfer MOS transistor unit TX, floating diffusion unit FD, first MOS structure unit MOS1, and second MOS structure unit MOS2. Referring to Figs. 23A to 23C, the transfer MOS transistor is ON, and the energy level is lower than the level of the photodiode PD, so all charges accumulated in the photodiode PD can be transferred to the FD region. The potential of the FD region is reset to VDD - Vth (Vth is the amount of voltage drop between the source and drain by the transfer MOS transistor) by the reset MOS transistor MRES (not shown).

When the staircase potential structure (FD and MOS structure units) is formed, and the amount of signal charges accumulated in the photodiode unit (PD) is small (light amount is small), as shown in Fig. 23A, the signal charges are transferred to the deep portion of the potential well. At this time, a floating diffusion voltage VFD is high, an accumulated signal charge amount Q is small (Fig. 24A), a capacitance Cap is small (Fig. 24B), the change rate of the output with respect to the light amount is high, and the sensitivity is high (Fig. 24C).

As shown in Figs. 23B and 23C, as the amount of

signal charges accumulated in the photodiode unit (PD) increases, the signal charges are also transferred to shallow portions of the staircase potential structure of the MOS structure units (MOS1, MOS2) stepwise. The floating diffusion voltage VFD becomes low, the accumulated signal charge amount Q increases (Fig. 24A), the capacitance Cap increases stepwise (Fig. 24B), the change rate of the output with respect to the light amount becomes low, and the sensitivity becomes low (Fig. 24C). In this way, the sensitivity can be changed in correspondence with the transferred signal charge amount.

As shown in Figs. 25A to 25C, an inverted "U"-shaped potential structure may be formed. This potential structure can be obtained by series-connecting the MOS capacitances.

In this case, when the amount of signal charges accumulated on the photodiode unit (PD) is small, the signal charges are transferred to the potential well of the FD region, as shown in Fig. 25A. As the amount of signal charges accumulated in the photodiode unit increases, the signal charges are transferred to the potential well formed by the MOS capacitance of the MOS structure unit MOS2, as shown in Fig. 25B. As the amount of signal charges further increases, the signal charges are transferred to the MOS capacitance of the MOS structure unit MOS1, as shown in Fig. 25C.

Fig. 26A shows the VFD (floating diffusion voltage) vs. signal charge amount characteristics at this time. Fig. 26B shows the VFD vs. Cap characteristics. Fig. 26C shows the light amount vs. output characteristics (sensitivity characteristics). Symbols a, b, and c in Figs. 26A to 26C denote the characteristics corresponding to the operative states shown in Figs. 25A to 25C, respectively.

In this embodiment, the staircase potential structure and inverted "U"-shaped potential structure have been described. However, the present invention is not limited to these potential structures.

Figs. 27 and 28 are schematic plan views of solid-state image pickup apparatuses having the above MOS capacitance.

Referring to Figs. 27 and 28, each solid-state image pickup apparatus has a photodiode (PD) 11, gate 12 of a transfer MOS transistor, floating diffusion region (FD) 13, gate 14 of a reset MOS transistor, and gate electrodes 15 and 16 for forming a MOS capacitance.

The ninth embodiment will be described below in which the staircase potential structure in Figs. 23A to 23C or inverted "U"-shaped potential structure in Figs. 25A to 25C is formed using not the MOS capacitance but buried p-n junction.

Fig. 29 is a schematic sectional view showing an

FD region and buried p-n junction. The structure shown in Fig. 29 has an FD region 21, heavily doped p-type surface region (PSR) 22, n-type diffusion region (DN) 26 that forms p-n junction with the PSR 22, and p-type well region (PWL) 25 that forms p-n junction with the n-type diffusion region 26 (DN). When a reverse bias voltage is applied to the p-n junction portion, a depletion layer extends. As shown in Fig. 29, there are a depletion layer extending from the p-n junction portion between the PSR 22 and n-type diffusion region DN 26 (depletion layer width a) and a depletion layer extending from the p-n junction portion between the n-type diffusion region DN 26 and PWL 25 (depletion layer width b). As the two depletion layers extend, all charges in the depletion layers are removed. For this reason, the charges are not accumulated, and the capacitance becomes small. When the reverse bias voltage becomes high to bring the depletion layers into contact with each other ($w = a + b$; w is the depth of the n-type diffusion region DN 26), and the capacitance of this portion almost disappears. Hence, as shown in Fig. 30, when a floating diffusion voltage VFD is high, and a reverse bias voltage VR is high, the capacitance is formed almost only by a capacitance CFD of the FD region. However, when the floating diffusion voltage VFD becomes low, and the reverse bias voltage VR becomes lower than a threshold voltage V1, the

depletion layer width (a + b) becomes smaller than the depth w. A capacitance CBPN of the buried p-n junction portion is added to the capacitance CFD. The threshold voltage V1 can be arbitrarily changed by changing the impurity concentration or depth w of the n-type diffusion region. When another n-type diffusion region is formed by changing the impurity concentration or width w of the n-type diffusion region, the staircase potential structure shown in Figs. 23A to 23C or inverted "U"-shaped potential structure shown in Figs. 25A to 25C can be formed.

Fig. 31 is a schematic sectional view showing an FD region and buried p-n junction when a staircase potential structure or inverted "U"-shaped potential structure is to be formed. The structure shown in Fig. 31 has an FD region 21, heavily doped p-type surface region (PSR) 22, n-type diffusion regions (DN1, DN2) 23 and 24 that form a p-n junction with the PSR 22, and p-type well region (PWL) 25. The n-type diffusion regions 23 and 24 are set at different impurity densities. The impurity densities are appropriately set to form the staircase potential structure or inverted "U"-shaped potential structure. To form the staircase potential structure, the n-type diffusion regions can be connected in series or parallel. To form the inverted "U"-shaped potential structure, the n-type diffusion regions are connected

in series. Instead of or in addition to changing the impurity concentration, the depth w of the n-type diffusion region may be changed.

Fig. 32 is a schematic plan view of a solid-state image pickup apparatus having the above buried p-n junction. The same reference numerals as in Fig. 27 denote the same members in Fig. 32. The structure shown in Fig. 32 has p-n junction portions 21 to 23.

The threshold voltage V1 can be arbitrarily changed by changing not only the impurity concentration or depth w of the n-type diffusion region but also the planar shape (e.g., width) of the n-type diffusion region.

The DN region 26 in Fig. 29 has the p-type region only in the vertical direction at the portion close to the FD region 21. A portion close to the distal end comes into contact with the p-type region even at the side surface of the DN region 26 and therefore is readily depleted. That is, the n-type diffusion region is readily depleted at a portion near the side surface. For this reason, when the width of the n-type diffusion region is small, the threshold voltage V1 becomes low due to the influence of the p-n junction portion at the side surface.

Fig. 34 shows the planar shape of the n-type diffusion region when an inverted "U"-shaped potential structure shown in Figs. 25A to 25C is formed. Fig. 33

shows the planar shape of the n-type diffusion region when the voltage vs. capacitance characteristics shown in Fig. 47 are obtained. In an n-type diffusion region DN1 shown in Fig. 33, a width d2 of a region close to the distal end portion is smaller than a width d1 of a region close to the FD region 5. The region close to the distal end portion is readily depleted (the depletion voltage is lower). In the n-type diffusion region DN1 shown in Fig. 34, the width d2 of the narrow portion is smaller than the width d1 of the region close to the FD region. The narrow region is readily depleted.

In the above-described eighth and ninth embodiments, signal charges are transferred by fixing the reset voltage at a predetermined potential (VDD). In the 10th embodiment, the sensitivity can be switched by appropriately changing the reset voltage.

The operation of a solid-state image pickup apparatus according to the present invention will be described first with reference to Figs. 35 and 36A to 36D. Fig. 35 is a schematic view of a solid-state image pickup apparatus including a reset MOS transistor. Figs. 36A to 36D are potential charts showing the light accumulation operation, reset operation, noise read-out operation, and signal transfer/signal read-out operation, respectively.

As shown in Fig. 36A, in a state wherein a

transfer transistor MTX and reset MOS transistor MRES are OFF, light is incident on a photodiode PD, and optical signal charges are accumulated.

Next, as shown in Fig. 36B, the reset MOS transistor MRES is turned on to reset the FD region. The reset voltage is VDD. The FD region is set at a potential (VDD - Vth). Signal charges overflowed from the photodiode are drained through the reset MOS transistor MRES.

As shown in Fig. 36C, the reset MOS transistor MRES is turned off to read out a noise signal.

Next, as shown in Fig. 36D, the transfer transistor MTX is turned on to transfer the signal charges from the photodiode PD to the FD region. The signal charges are read out as a voltage signal. The previously readout noise signal is subtracted from the voltage signal to obtain a signal without any noise.

In this solid-state image pickup apparatus, the sensitivity can be changed by appropriately changing the reset potential. A case wherein the FD region and MOS structure units have a staircase potential structure will be described below.

For example, when the reset voltage is VRES1 (= VDD), signal charges are accumulated in the deep portion of the potential well of the FD region, as shown in Fig. 37A. On the other hand, when the reset voltage is VRES2 (< VRES1), signal charges are

accumulated in a shallower portion of the potential well formed from the FD region and MOS structure unit MOS1, as shown in Fig. 37B. That is, when the reset voltage is made low, charges corresponding to the reset voltage are accumulated in the deep portion of the potential well of the FD region, so the signal charges are accumulated in a larger capacitance state. For this reason, when the reset voltage is controlled, the sensitivity can be switched. Fig. 38 is a graph showing the light amount vs. output characteristics (sensitivity characteristics). Referring to Fig. 38, a represents the characteristics when the reset voltage is VRES1, and b represents the characteristics when the reset voltage is VRES2.

A reset voltage application method for a case wherein pixels each constructed by the above solid-state image pickup apparatus are arrayed in a matrix will be described below. The members of the pixel to be described below are the same as in Fig. 1.

To set the same sensitivity for all pixels, a predetermined reset voltage is applied to all pixels. In this case, as shown in Fig. 39, the sources of the transfer MOS transistors MRES of all pixels are connected to a voltage source for supplying the reset voltage VRES.

To arbitrarily set the sensitivity in units of pixels, an arbitrary reset voltage is set and applied

in units of pixels. In this case, the reset voltage is applied in units of columns, and the pixels are scanned in units of rows. For the pixel shown in Fig. 40, a power supply line for reset voltage application is prepared for each column, the sources of the transfer MOS transistors MRES of one column are commonly connected, and the reset signal is applied to the gates of the transfer MOS transistors MRES of each row, thereby applying an arbitrary reset voltage in units of pixels. For the pixel shown in Fig. 41, the power supply line for reset voltage application is also used as an output signal line. The reset operation and signal read-out operation are performed at different timings. Hence, when the output signal line and the source of the transfer MOS transistor MRES are connected, and the reset signal is applied to the gates of the transfer MOS transistors MRES of each row, an arbitrary reset voltage can be applied in units of pixels.

In this embodiment, the sensitivity can be switched by changing the reset voltage. Hence, a solid-state image pickup apparatus which samples the light amount incident on a pixel in advance and sets the reset voltage in accordance with the sampling result can be constructed. In the pixel structure shown in Fig. 39, the reset voltage is changed for all pixels. In the pixel structures shown in Figs. 40 and

41, the reset voltage can be changed for some pixels.

Fig. 42 is a block diagram of a camera apparatus using a solid-state image pickup apparatus which sets the reset voltage in accordance with a sampling result. Referring to Fig. 42, the apparatus has a solid-state image pickup element (sensor) 31 capable of arbitrarily setting the reset voltage, CDS (correlation double sampling circuit)/AGC (automatic gain controller) 32, A/D converter 33, camera signal processing IC 34 for processing a signal and outputting it as, e.g., an NTSC signal, and saturation bit memory 35.

In this camera apparatus, when an input has a predetermined value or more, the camera signal processing IC 34 determines that the signal is saturated. In accordance with the determination result, the saturation bit is stored in the saturation bit memory 35, and the saturation bit signal is input to the sensor 31. It is determined on the basis of this saturation bit signal whether the pixel is saturated. The reset voltage is controlled in accordance with the determination result (in this case, a signal one frame ahead is used as a sampling signal).

As shown in Fig. 43, during the signal charge accumulation period, the reset MOS transistor MRES is turned off to accumulate a signal that has overflowed from the photodiode PD onto the FD region, i.e., an overflow drain (OFD) signal (or a smear signal).

Saturation is determined on the basis of this signal as a sampling signal. The reset voltage can be switched in accordance with the determination result before signal charge transfer. In this case, saturation determination can be performed in the sensor chip.

Additionally, before signal charge accumulation, a signal accumulated in a short accumulation period is transferred from the photodiode PD to the FD region. This signal is held on the FD region during the accumulation period. Before reading the signal charges, the signal held on the FD region is read out as a sampling signal, and saturation is determined. The reset voltage is switched on the basis of the determination result. In this case, saturation determination can be performed in the sensor chip.

The structure of an area sensor having the above-described pixel cells arrayed in a matrix will be described next.

Fig. 44 is a schematic view showing the structure of the area sensor. As shown in Fig. 44, rows of pixel cells arrayed in a matrix are scanned by a vertical scanning circuit 100. Signals ϕRES, ϕTX, and ϕSEL are sent in units of rows. Noise and sensor signals are output to the vertical output lines and accumulated in noise signal accumulation capacitances and sensor signal accumulation capacitances, which are connected to the vertical output lines via switching MOS

transistors, in units of rows. The noise signals and sensor signals accumulated in the capacitance are scanned by a horizontal scanning circuit 101 in units of columns. A noise signal N and sensor signal S are sequentially sent to the inverting input terminal (-) and noninverting input terminal (+) of a differential amplifier A in units of columns through the horizontal output lines. The differential amplifier A executes subtraction to obtain the signal S - N for each pixel. MOS transistors MCHR1 and MCHR2 for resetting the horizontal output lines to predetermined potentials are controlled by a signal φCHR. Signals φTN and φTS control the switching MOS transistors for transferring the noise and sensor signals to the capacitances.

Fig. 45 is a block diagram showing the arrangement of a solid-state image pickup apparatus according to the 11th embodiment of the present invention. Fig. 46 is a timing chart showing the operation of the solid-state image pickup apparatus.

In this embodiment, signals are read out by the following read-out method using a circuit which temporarily holds, in a signal holding unit, a noise signal from the same sensor unit as in the above-described embodiments and a noise signal + optical signal and then reads out the signals.

(1) As shown in Fig. 46, the reset switch (reset MOS transistor MRES) is turned off during the accumulation

period before the signal read-out.

(2) Before reading the noise signal, a light amount sampling signal as a signal corresponding to the incident light amount accumulated in the FD region is read out ((1) in Fig. 46). As this signal, an optical signal entering the FD region is used. In the CCD, such an optical signal is prevented by layout or light shielding. In this embodiment, however, this optical signal is actively used to obtain the light amount sampling signal. When the upper portion of the FD region is opened to receive a larger signal, as needed, a larger sampling signal can be obtained.

(3) After the reset switch is turned on/off to reset the FD region, the noise signal is read out ((2) in Fig. 46).

(4) Using the signal (1) or signals (1) and (2) in Fig. 46, the incident light amount is determined in the reset voltage control circuit, and an appropriate reset voltage is set in accordance with the determination result.

(5) The reset voltage determined in (4) is set to reset the FD region again. Of voltages V1 to V4 shown in Fig. 46, the voltage V2 is selected as the reset voltage.

(6) The noise signal is read out after resetting ((3) in Fig. 46).

(7) The transfer switch (transfer transistor MTX) is

turned on/off by a transfer pulse to transfer signal charges from the photodiode to the FD region and read out the noise + optical signal ((4) in Fig. 46). The main read-out of an image signal is performed using the signals (3) and (4) in Fig. 46.

As described above, in this embodiment, the sensitivity is controlled by the reset voltage in accordance with the light amount using the sampling signal, thereby obtaining a variety of image signals.

The solid-state image pickup apparatuses of the above-described eighth to 11th embodiments can be used not only for an area sensor but also for a line sensor.

As described above, according to the eighth to 11th embodiments, the sensitivity can be changed in correspondence with the signal charges accumulated in the photoelectric conversion unit, and a signal with wide dynamic range can be obtained.

The sensitivity can be switched by appropriately changing the reset voltage.

For this reason, a signal having high sensitivity but narrow dynamic range and a signal having low sensitivity but wide dynamic range can be selectively output, as needed. Hence, the solid-state image pickup apparatuses of the eighth to 11th embodiments can be used for, e.g., back light correction.

Fig. 48 is a block diagram showing, as the 12th embodiment of the present invention, a video camera

apparatus using one of the solid-state image pickup apparatuses of the first to sixth and eighth to 11th embodiments.

Referring to Fig. 48, the video camera apparatus has a lens system 1, iris 2, motors 3, 5, and 7, magnification lens driving unit 4 for controlling the motor 3, iris mechanism driving unit 6 for controlling the motor 5 to drive the iris 2, and focus compensation lens driving unit 8 for controlling the motor 7. As a solid-state image pickup element 9 for photoelectrically converting an optical signal input from the lens system 1, the solid-state image pickup apparatus of this embodiment shown in Fig. 18 is used. A signal (S2 - N1) or signal (S1 - N2) is output in accordance with the output selection signal from a microcomputer 15. The apparatus also has a CDS/AGC (correlation double sampling/automatic gain control) 10, and A/D converter 11. A camera signal processing circuit 12 has a Y/C separation circuit 12a, luminance signal processing circuit 12b, chrominance signal processing circuit 12c, chrominance suppression circuit 12d, digital output conversion circuit 12e, and saturated pixel discrimination circuit 12f. The saturated pixel discrimination circuit 12f determines a saturated pixel on the basis of the luminance and chrominance signals. The saturated pixel determination result is input to the microcomputer 15, and the output

selection signal is output on the basis of the determination result. The microcomputer 15 controls the magnification lens driving unit 4, iris mechanism driving unit 6, and focus compensation lens driving unit 8 on the basis of the signal from the camera signal processing circuit 12.

The output from the camera signal processing circuit 12 is sent to a monitor unit 14 through a digital decoder and D/A converter 13 for image display and also sent to a VTR.

Fig. 49 is a block diagram showing a conventional video camera apparatus. This apparatus is different from this embodiment in that the saturated pixel discrimination circuit 12f is not arranged, and no output selection signal is output.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.